Hit List

Search Results - Record(s) 1 through 15 of 15 returned.

☐   1.   Document ID: US 20020023202 A1

Using default format because multiple data bases are involved.

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L2: Entry 1 of 15                        File: PGPB            Feb 21, 2002


PGPUB-DOCUMENT-NUMBER: 20020023202
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020023202 A1


TITLE: Load value queue input replication in a simultaneous and redundantly
threaded processor


PUBLICATION-DATE: February 21, 2002


INVENTOR-INFORMATION:
NAME                              CITY          STATE   COUNTRY     RULE-47
Mukherjee, Shubhendu S.           Framingham    MA      US


US-CL-CURRENT: 712/225
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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   2.   Document ID: US 20010037448 A1

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L2: Entry 2 of 15                        File: PGPB            Nov 1, 2001


PGPUB-DOCUMENT-NUMBER: 20010037448
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037448 A1


TITLE: Input replicator for interrupts in a simultaneous and redundantly threaded
processor


PUBLICATION-DATE: November 1, 2001


INVENTOR-INFORMATION:
NAME                              CITY          STATE   COUNTRY     RULE-47
Mukherjee, Shubhendu S.           Framingham    MA      US
Reinhardt, Steven K.              Ann Arbor     MI      US


US-CL-CURRENT: 712/244; 712/245
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h   e b   b g e e e f   e   e   ef   b   e

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 3.   Document ID: US 20010037447 A1

L2: Entry 3 of 15   File: PGPB   Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010037447
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037447 A1

TITLE: Simultaneous and redundantly threaded processor branch outcome queue

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

US-CL-CURRENT: 712/239; 712/235

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 4.   Document ID: US 20010037445 A1

L2: Entry 4 of 15   File: PGPB   Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010037445
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037445 A1

TITLE: Cycle count replication in a simultaneous and redundantly threaded processor

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	

US-CL-CURRENT: 712/216; 712/245

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 5.   Document ID: US 20010034854 A1

L2: Entry 5 of 15   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034854
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034854 A1

h   e b   b g e e e f   e   e   ef   b   e

TITLE: Simultaneous and <u>redundantly threaded</u> processor uncached load address comparator and data value <u>replication</u> circuit

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	

US-CL-CURRENT: <u>714</u>/<u>5</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 6. Document ID: US 20010034827 A1

L2: Entry 6 of 15   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034827
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034827 A1

TITLE: Active load address buffer

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

US-CL-CURRENT: <u>712</u>/<u>225</u>; <u>711</u>/<u>126</u>, <u>712</u>/<u>216</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 7. Document ID: US 20010034824 A1

L2: Entry 7 of 15   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034824
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034824 A1

TITLE: Simultaneous and <u>redundantly threaded</u> processor store instruction comparator

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

h   e b   b g e e f   e   e   ef   b   e

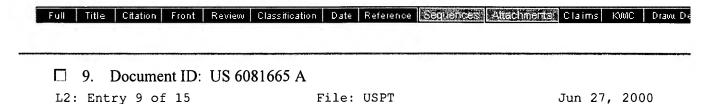US-CL-CURRENT: <u>712</u>/<u>215</u>; <u>712</u>/<u>218</u>, <u>712</u>/<u>225</u>, <u>712</u>/<u>23</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 8. Document ID: US 6598122 B2

L2: Entry 8 of 15   File: USPT   Jul 22, 2003

US-PAT-NO: 6598122
DOCUMENT-IDENTIFIER: US 6598122 B2

TITLE: Active load address buffer

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 9. Document ID: US 6081665 A

L2: Entry 9 of 15   File: USPT   Jun 27, 2000

US-PAT-NO: 6081665
DOCUMENT-IDENTIFIER: US 6081665 A

TITLE: Method for efficient soft real-time execution of portable byte code computer programs

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 10. Document ID: US 5890189 A

L2: Entry 10 of 15   File: USPT   Mar 30, 1999

US-PAT-NO: 5890189
DOCUMENT-IDENTIFIER: US 5890189 A

TITLE: Memory management and protection system for virtual memory in computer system

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 11. Document ID: US 5627987 A

L2: Entry 11 of 15   File: USPT   May 6, 1997

US-PAT-NO: 5627987
DOCUMENT-IDENTIFIER: US 5627987 A

TITLE: Memory management and protection system for virtual memory in computer system

h   e b   b g e e e f   e   e   ef   b   e

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐   12.   Document ID: US 20020023202 A1

L2: Entry 12 of 15   File: DWPI   Feb 21, 2002

DERWENT-ACC-NO: 2002-280028
DERWENT-WEEK: 200232
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TITLE: Computer system for space applications, has pipelined simultaneous and
redundantly threaded processor to execute instructions in leading thread and
redundant trailing thread

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐   13.   Document ID: US 20010037445 A1

L2: Entry 13 of 15   File: DWPI   Nov 1, 2001

DERWENT-ACC-NO: 2002-017169
DERWENT-WEEK: 200232
COPYRIGHT 2004 DERWENT INFORMATION LTD

TITLE: Computer system for mission critical multitasking has simultaneous-
redundantly threaded processor to replicate counter value for related command in
trailing thread when cycle count read command appears in leading thread

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐   14.   Document ID: US 6598122 B2, US 20010034827 A1

L2: Entry 14 of 15   File: DWPI   Jul 22, 2003

DERWENT-ACC-NO: 2002-105519
DERWENT-WEEK: 200356
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TITLE: Simultaneous and redundantly threaded processor for computer system used in
mission-critical applications, increments or decrements slack counter based on
execution of load instruction of leading or trailing thread

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐   15.   Document ID: US 20010034854 A1

L2: Entry 15 of 15   File: DWPI   Oct 25, 2001

DERWENT-ACC-NO: 2002-040692
DERWENT-WEEK: 200232

h   e b   b g ee e f   e   e   ef   b   e

TITLE: Computer system allows execution of memory request and initiates fault
recovery based on comparison result that indicates whether each corresponding
memory request generated by threads of microprocessor matches

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

| Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS |

Term	Documents
DUPLICAT$4	0
DUPLICAT	1082
DUPLICATA	15
DUPLICATABL	1
DUPLICATABLE	180
DUPLICATABLY	1
DUPLICATABL6	1
DUPLICATAE	1
DUPLICATANG	1
DUPLICATA-D	2
(L1 AND (DUPLICAT$4 OR REPLICAT$4 OR COP$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	15

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Display Format: | - | Change Format

Previous Page   Next Page   Go to Doc#

h   e b   b g e e e f   e   e   ef   b   e

Hit List

Search Results - Record(s) 1 through 12 of 12 returned.

☐ 1. Document ID: US 20020023202 A1

Using default format because multiple data bases are involved.

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L6: Entry 1 of 12                    File: PGPB              Feb 21, 2002


PGPUB-DOCUMENT-NUMBER: 20020023202
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020023202 A1


TITLE: Load value queue input replication in a simultaneous and redundantly
threaded processor


PUBLICATION-DATE: February 21, 2002


INVENTOR-INFORMATION:
NAME                             CITY          STATE    COUNTRY     RULE-47
Mukherjee, Shubhendu S.          Framingham    MA       US


US-CL-CURRENT: 712/225
```

☐ 2. Document ID: US 20010037448 A1

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L6: Entry 2 of 12                    File: PGPB              Nov 1, 2001


PGPUB-DOCUMENT-NUMBER: 20010037448
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037448 A1


TITLE: Input replicator for interrupts in a simultaneous and redundantly threaded
processor


PUBLICATION-DATE: November 1, 2001


INVENTOR-INFORMATION:
NAME                             CITY          STATE    COUNTRY     RULE-47
Mukherjee, Shubhendu S.          Framingham    MA       US
Reinhardt, Steven K.             Ann Arbor     MI       US


US-CL-CURRENT: 712/244; 712/245
```

h   e b   b g e e f   e   e   ef   b   e

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐ 3.   Document ID: US 20010037447 A1

L6: Entry 3 of 12   File: PGPB   Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010037447
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037447 A1

TITLE: Simultaneous and redundantly threaded processor branch outcome queue

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

US-CL-CURRENT: 712/239; 712/235

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐ 4.   Document ID: US 20010037445 A1

L6: Entry 4 of 12   File: PGPB   Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010037445
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010037445 A1

TITLE: Cycle count replication in a simultaneous and redundantly threaded processor

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	

US-CL-CURRENT: 712/216; 712/245

`Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De`

☐ 5.   Document ID: US 20010034854 A1

L6: Entry 5 of 12   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034854
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034854 A1

h   e b   b g e e e f   e   e   ef   b   e

TITLE: Simultaneous and redundantly threaded processor uncached load address comparator and data value replication circuit

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	

US-CL-CURRENT: 714/5

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 Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De
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☐ 6.   Document ID: US 20010034827 A1

L6: Entry 6 of 12   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034827
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034827 A1

TITLE: Active load address buffer

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

US-CL-CURRENT: 712/225; 711/126, 712/216

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 Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De
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☐ 7.   Document ID: US 20010034824 A1

L6: Entry 7 of 12   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034824
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034824 A1

TITLE: Simultaneous and redundantly threaded processor store instruction comparator

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mukherjee, Shubhendu S.	Framingham	MA	US	
Reinhardt, Steven K.	Ann Arbor	MI	US	

h   e b   b g e e e f   e   e   ef   b   e

US-CL-CURRENT: <u>712</u>/<u>215</u>; <u>712</u>/<u>218</u>, <u>712</u>/<u>225</u>, <u>712</u>/<u>23</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 8.   Document ID: US 6598122 B2

L6: Entry 8 of 12   File: USPT   Jul 22, 2003

US-PAT-NO: 6598122
DOCUMENT-IDENTIFIER: US 6598122 B2

TITLE: Active load address buffer

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 9.   Document ID: US 5610413 A

L6: Entry 9 of 12   File: USPT   Mar 11, 1997

US-PAT-NO: 5610413
DOCUMENT-IDENTIFIER: US 5610413 A

TITLE: Group II-VI compound semiconductor light emitting devices and an ohmic
contact therefor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 10.   Document ID: US 5548137 A

L6: Entry 10 of 12   File: USPT   Aug 20, 1996

US-PAT-NO: 5548137
DOCUMENT-IDENTIFIER: US 5548137 A

TITLE: Group II-VI compound semiconductor light emitting devices and an ohmic
contact therefor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 11.   Document ID: US 5088036 A

L6: Entry 11 of 12   File: USPT   Feb 11, 1992

US-PAT-NO: 5088036
DOCUMENT-IDENTIFIER: US 5088036 A

TITLE: Real time, concurrent garbage collection system and method

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

h   e   b   b   g e e f   e   e   ef   b   e

☐   12.   Document ID: US 20010037445 A1

L6: Entry 12 of 12   File: DWPI   Nov 1, 2001

DERWENT-ACC-NO: 2002-017169
DERWENT-WEEK: 200232
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TITLE: Computer system for mission critical multitasking has simultaneous-
redundantly threaded processor to replicate counter value for related command in
trailing thread when cycle count read command appears in leading thread

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

| Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS |

Term	Documents
DUPLICAT$4	0
DUPLICAT	1082
DUPLICATA	15
DUPLICATABL	1
DUPLICATABLE	180
DUPLICATABLY	1
DUPLICATABL6	1
DUPLICATAE	1
DUPLICATANG	1
DUPLICATA-D	2
(L4 AND (DUPLICAT$4 OR REPLICAT$4 OR COP$3) NEAR5 (CLOCK$1 OR CYCLE$1)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	12

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Previous Page   Next Page   Go to Doc#

h   e b   b g ee e f   e   e   ef   b   e